FORM PTO-1449 U.S. Department of Commerce
Patent and Trademark Office

LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)

Attorney Docket Number	Serial No.
5646-103	10/671,305
Applicants: Fang et al.	
Filing Date: September 24, 2003	Group ~~2817~~ 2816

U. S. PATENTS & PATENT APPLICATION PUBLICATIONS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
JL	1	6,539,072	03-25-03	Donnelly et al.	375	371	
JL	2	6,125,157	09-26-00	Donnelly et al.	375	371	
JL	3	5,614,855	03-25-97	Lee et al.	327	158	
JL	4	5,485,490	5,485,490	Leung et al.	375	371	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes | No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JL	5	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496

EXAMINER JL DATE CONSIDERED 3/28/2005

*EXAMINER Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/671,305
Filing Date	September 24, 2003
First Named Inventor	Al Fang
Group Art Unit	~~2817~~ 2816
Examiner Name	~~To Be Assigned~~ T. LAM
Attorney Docket Number	5646-103

U.S. PATENTS AND PATENT PUBLICATIONS

Examiner Initials*	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document Office	Foreign Patent Document Number	Foreign Patent Document Kind Code (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	T

OTHER NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
	1	Pixel-Flow System Documentation, Rev. 0006.0, Chapter IV.9 Clock Input Buffer and Delay-Locked Loop (January 23, 2001)	
	2	Efendovich et al., "Multifrequency Zero-Jitter Delay-Locked Loop," IEEE Journal of Solid-State Circuits, Vol. 29, No. 1, January 1994, pp. 67-70	
	3	Bazes, Mel, "An Interpolating Clock Synthesizer," IEEE Journal of Solid-State Circuits, Vol. 31, No. 9, September 1996, pp. 1295-1301	
	4	Lin et al., "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4, April 1999, pp. 565-568	
	5	Garlepp et al, "A Portable Digital DLL for High-Speed CMOS Interface Circuits," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp. 632-644	
	6	Maneatis et al., "Precise Delay Generation Using Coupled Oscillators," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, pp. 1273-1282	
	7	Sidiropoulos et al., "A Semidigital Dual Delay-Locked Loop," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1683-1692	
	8	Sidiropoulos et al., "SA 20.2: A Semi-Digital DLL with Unlimited Phase Shift Capability and 0.08-400MHz Operating Range," 1997 IEEE International Solid-State Circuits Conference Proceedings, 10 pages	

Examiner Signature		Date Considered	3/28/2005

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